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09/737,301	12/14/2000	David Brian Zaun	80113-0166(D2396)	1732
20480 7590 01/19/2007 STEVEN L. NICHOLS RADER, FISHMAN & GRAVER PLLC 10653 S. RIVER FRONT PARKWAY SUITE 150 SOUTH JORDAN, UT 84095			EXAMINER RYMAN, DANIEL J	
			ART UNIT 2616	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.		Applicant(s)	
	09/737,301		ZAUN ET AL.	
	Examiner		Art Unit	
	Daniel J. Ryman		2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25, 27-33 and 35-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25, 27-33 and 35-45 is/are rejected.
- 7) ☒ Claim(s) 3 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. The indicated allowability of claims 1-26, 28-33, and 34-45 (as amended to include previously indicated allowable subject matter) is withdrawn in view of the newly discovered reference(s) to Slattery et al. (USPN 6,111,896), Anderson et al. (USPN 5,905,713), Van Den Heuvel (USPN 6,175,577), Komi et al. (USPN 6,477,185), and Magee et al. (USPN 6,002,687). Rejections based on the newly cited reference(s) follow.

Claim Objections

2. Claim 3 is objected to because of the following informalities: in line 2 “a input” should be “an input”. Appropriate correction is required.
3. Claim 20 is objected to because of the following informalities: in line 2 “a input” should be “an input”. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3, 4, 6, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Slattery et al. (USPN 6,111,896).
6. Regarding claim 1, Slattery discloses an input processing device for use in a re-multiplexing module that processes input packet data, comprising: an input interface that

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receives a plurality of data transport streams each of which contains input packet data (where the remultiplexer shown in Figs. 1 and 2 receives a plurality of data transport streams, col. 12, lines 58-65, at an interface that “selectively extracts only particular ones of the transport packets from a TS,” col. 9, lines 49-52, and where the transport streams each contain input packet data, col. 3, lines 44-45); a corresponding plurality of input processors coupled to the input interface to receive input packet data from a respective data transport stream (where each input port has an adapter, i.e. input processor, see Fig. 2, which contains a data link control circuit, col. 17, lines 59-64, where the data link control circuit receives input packet data from a respective data transport stream, col. 15, lines 32-39); and a corresponding plurality of packet identifier tables each of which is coupled to a respective input processor (Fig. 2 and col. 14, lines 54-64, where each input port also has a cache which stores a PID filter map, i.e. packet identifier table, which the data link control circuit uses to determine which transport packets to retain, see also col. 15, lines 32-39).

7. Regarding claim 3, Slattery discloses that each input processor includes an input processor control logic portion that validates the input packet data (col. 15, lines 32-39, where the adapter, i.e. the input processor, includes a data link control circuit, i.e. input processor control logic portion, which determines which transport packets to retain, i.e. validates the input packet data).

8. Regarding claim 4, Slattery discloses that each input processor control logic portion validates the input packet data by extracting a packet identifier number from a header in the input packet data and checking the packet identifier number with the corresponding packet identifier table (col. 15, lines 32-39, where “the data link control circuit 112 filters out and retains only

selected transport packets received from the incoming TS as specified in a downloadable filter map,” and where the filter map is a PID filter map, col. 15, line 64-col. 16, line 2).

9. Regarding claim 6, Slattery discloses that each input processor includes a data delay register that delays the input packet data before the input processor writes data to a packet buffer (where the adapter stores the packets in a cache, i.e. a delay register, col. 15, lines 39-43, before the packets are passed to a host memory, col. 15, lines 16-21, which contains a buffer, col. 16, lines 16-20, see also col. 14, lines 47-50).

10. Regarding claim 8, Slattery discloses that each input processor includes a host processor interface (col. 15, lines 61-64, where the adapter, i.e. input processor, communicates with a host processor, ref. 160, such that the adapter includes a host processor interface).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 2, 5, 7, 11, 14-18, 20, 21, 23, 24, 27, 29, 30, 32, 33, 35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slattery et al. (USPN 6,111,896).

13. Regarding claim 2, Slattery discloses an input processing device for use in a re-multiplexing module that processes input packet data, comprising: an input interface that receives the input packet data (where the remultiplexer shown in Figs. 1 and 2 receives a plurality of data transport streams, col. 12, lines 58-65, at an interface that “selectively extracts only particular ones of the transport packets from a TS,” col. 9, lines 49-52, and where the

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transport streams each contain input packet data, col. 3, lines 44-45); an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer (where each input port has an adapter, i.e. input processor, see Fig. 2, which contains a data link control circuit, col. 17, lines 59-64, where the data link control circuit receives input packet data from a respective data transport stream, col. 15, lines 32-39, and which writes data to a host memory, col. 15, lines 16-19, containing a packet buffer, col. 16, lines 16-20); and a packet identifier table coupled to the input processor (Fig. 2 and col. 14, lines 54-64, where each input port also has a cache which stores a PID filter map, i.e. packet identifier table, which the data link control circuit uses to determine which transport packets to retain, see also col. 15, lines 32-39).

Slattery does not expressly disclose that the input processor includes a serial-to-parallel converter for converting the input packet data received from the input interface. However, Examiner takes official notice that it is well known in the art to send data in parallel, which results in faster transfer rates, or serially, which results in lower costs due to fewer transfer lines, where one of ordinary skill in the art would choose one type of transfer over the other depending on system constraints. Examiner also takes official notice that serial-to-parallel converters are used in the art to enable a system to convert between serial and parallel data formats. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a serial-to-parallel converter in the input processor for converting input packet data received from the input interface in order to enable the input processor to convert data received into a format compatible with the input processor.

Slattery does not expressly disclose that the input processor checks a length of each packet of said packet data received and discards packets of incorrect length. However, Slattery does disclose that each transport packet is a fixed length (col. 3, lines 12-14). It is implicit that any packet arriving at the input processor that is a length other than the fixed length is a corrupted packet, i.e. the packet has been corrupted during transport, which has resulted in the packet having a length other than the given length. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor check a length of each received packet and to discard packets of an incorrect length in order to ensure that any corrupted packet is discarded.

14. Regarding claim 5, Slattery does not expressly disclose that each input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field. However, Slattery does disclose that each input processor obtains a reference time and records this time along with the packet (col. 15, lines 43-49). Slattery also discloses that the output processors check to see if packets have a valid PCR (col. 15, lines 56-60). Slattery further discloses that PCRs are crucial to proper recovery of the information stream (col. 3, lines 26-34). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor check the packet data for a valid program clock reference field to ensure that the system does not operate on a corrupted PCR, where a corrupted PCR could distort the decoded information stream.

15. Regarding claim 7, Slattery discloses an input processing device for use in a re-multiplexing module that processes input packet data, comprising: an input interface that receives the input packet data (where the remultiplexer shown in Figs. 1 and 2 receives a

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plurality of data transport streams, col. 12, lines 58-65, at an interface that “selectively extracts only particular ones of the transport packets from a TS,” col. 9, lines 49-52, and where the transport streams each contain input packet data, col. 3, lines 44-45); an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer (where each input port has an adapter, i.e. input processor, see Fig. 2, which contains a data link control circuit, col. 17, lines 59-64, where the data link control circuit receives input packet data from a respective data transport stream, col. 15, lines 32-39, and which writes data to a host memory, col. 15, lines 16-19, containing a packet buffer, col. 16, lines 16-20); and a packet identifier table coupled to the input processor (Fig. 2 and col. 14, lines 54-64, where each input port also has a cache which stores a PID filter map, i.e. packet identifier table, which the data link control circuit uses to determine which transport packets to retain, see also col. 15, lines 32-39); wherein the input processor includes a time reference generator that generates timestamp values for the input packet data (col. 15, lines 43-49, where the input processor records “receipt times,” i.e. timestamp values, for the input packet data).

Slattery does not expressly disclose that the input processor checks a length of each packet of said packet data received and discards packets of incorrect length. However, Slattery does disclose that each transport packet is a fixed length (col. 3, lines 12-14). It is implicit that any packet arriving at the input processor that is a length other than the fixed length is a corrupted packet, i.e. the packet has been corrupted during transport, which has resulted in the packet having a length other than the given length. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor check a

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length of each received packet and to discard packets of an incorrect length in order to ensure that any corrupted packet is discarded.

16. Regarding claim 11, Slattery discloses an input processing device for use in a remultiplexing module that processes input packet data, comprising: an input interface that receives the input packet data (where the remultiplexer shown in Figs. 1 and 2 receives a plurality of data transport streams, col. 12, lines 58-65, at an interface that “selectively extracts only particular ones of the transport packets from a TS,” col. 9, lines 49-52, and where the transport streams each contain input packet data, col. 3, lines 44-45); an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer (where each input port has an adapter, i.e. input processor, see Fig. 2, which contains a data link control circuit, col. 17, lines 59-64, where the data link control circuit receives input packet data from a respective data transport stream, col. 15, lines 32-39, and which writes data to a host memory, col. 15, lines 16-19, containing a packet buffer, col. 16, lines 16-20), an input processor control logic portion that receives data from the interface (col. 15, lines 32-34, where the data link control circuit, i.e. input processor control logic, receives data from the interface); a data delay register that delays the input packet data before the input processor writes data to the packet buffer (where the adapter stores the packets in a cache, i.e. a delay register, col. 15, lines 39-43, before the packets are passed to a host memory, col. 15, lines 16-21, which contains a buffer, col. 16, lines 16-20, see also col. 14, lines 47-50); a time reference generator that generates timestamp values for the input packet data (col. 15, lines 43-49, where the input processor records “receipt times,” i.e. timestamp values, for the input packet data); and a host processor interface (col. 15, lines 61-64, where the adapter, i.e. input processor,

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communicates with a host processor, ref. 160, such that the adapter includes a host processor interface); and a packet identifier table coupled to the input processor (Fig. 2 and col. 14, lines 54-64, where each input port also has a cache which stores a PID filter map, i.e. packet identifier table, which the data link control circuit uses to determine which transport packets to retain, see also col. 15, lines 32-39).

Slattery does not expressly disclose that the input processor includes a serial-to-parallel converter for converting the input packet data received from the input interface, where the serial-to-parallel converter is located prior to the input processor control logic. However, Examiner takes official notice that it is well known in the art to send data in parallel, which results in faster transfer rates, or serially, which results in lower costs due to fewer transfer lines, where one of ordinary skill in the art would choose one type of transfer over the other depending on system constraints. Examiner also takes official notice that serial-to-parallel converters are used in the art to enable a system to convert between serial and parallel data formats. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a serial-to-parallel converter in the input processor for converting input packet data received from the input interface in order to enable the input processor to convert data received into a format compatible with the input processor control logic.

Slattery does not expressly disclose that the input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field. However, Slattery does disclose that each input processor obtains a reference time and records this time along with the packet (col. 15, lines 43-49). Slattery also discloses that the output processors check to see if packets have a valid PCR (col. 15, lines 56-60). Slattery further

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discloses that PCRs are crucial to proper recovery of the information stream (col. 3, lines 26-34). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor check the packet data for a valid program clock reference field to ensure that the system does not operate on a corrupted PCR, where a corrupted PCR could distort the decoded information stream.

17. Regarding claim 14, Slattery discloses that the input packet data includes a plurality of packets (col. 3, lines 44-45, where the transport streams each contain input packet data), and wherein the input processor control logic portion validates the input packet data by extracting a packet identifier number from a header in the input packet data and checking the packet identifier number with the packet identifier table (col. 15, lines 32-39, where “the data link control circuit 112 filters out and retains only selected transport packets received from the incoming TS as specified in a downloadable filter map,” and where the filter map is a PID filter map, col. 15, line 64-col. 16, line 2).

18. Regarding claim 15, Slattery discloses that the input packet data includes a plurality of packets (col. 3, lines 44-45, where the transport streams each contain input packet data), and wherein the timestamp value generated by the time reference generator corresponds to a time period during which a packet passes through the re-multiplexing module (col. 15, lines 43-49, where the input processor records “receipt times,” i.e. timestamp values, for the input packet data, and where a receipt time corresponds to a time period during which a packet passes through the re-multiplexing module).

19. Regarding claim 16, Slattery does not expressly disclose that each input processor checks a length of each packet of said packet data received and discards packets of incorrect

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length. However, Slattery does disclose that each transport packet is a fixed length (col. 3, lines 12-14). It is implicit that any packet arriving at the input processor that is a length other than the fixed length is a corrupted packet, i.e. the packet has been corrupted during transport, which has resulted in the packet having a length other than the given length. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor check a length of each received packet and to discard packets of an incorrect length in order to ensure that any corrupted packet is discarded.

20. Regarding claims 17, 27 and 35, Slattery does not expressly disclose that, if the input processor discards a packet of incorrect length, an error bit is set that is readable by a host processor and indicates that a packet of incorrect length was discarded. However, Examiner takes official notice that it is well known in the art to signal to a processor when a packet has been discarded in order to permit the processor to collect error statistics. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor set an error bit that is readable by a host processor when it discards a packet of incorrect length in order to permit the processor to collect error statistics.

21. Regarding claim 18, Slattery discloses a corresponding plurality of packet buffers, wherein each input processor writes packets of packet data to a corresponding packet buffer if that packet has an identifier that matches an entry in the corresponding packet identifier table (col. 15, lines 16-31, where the cache, i.e. the PID table, contains storage locations).

22. Regarding claim 20, Slattery discloses that the input processor includes an input processor control logic portion that validates the input packet data using said packet identifier table (col. 15, lines 32-39, where the adapter, i.e. the input processor, includes a data link control

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circuit, i.e. input processor control logic portion, which determines which transport packets to retain, i.e. validates the input packet data, using the PID filter map, see also col. 15, line 64-col. 16, line 2).

23. Regarding claims 21 and 30, Slattery does not expressly disclose that the input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field. However, Slattery does disclose that each input processor obtains a reference time and records this time along with the packet (col. 15, lines 43-49). Slattery also discloses that the output processors check to see if packets have a valid PCR (col. 15, lines 56-60). Slattery further discloses that PCRs are crucial to proper recovery of the information stream (col. 3, lines 26-34). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor check the packet data for a valid program clock reference field to ensure that the system does not operate on a corrupted PCR, where a corrupted PCR could distort the decoded information stream.

24. Regarding claims 23 and 32, Slattery discloses that the input processor includes a data delay register that delays the input packet data before the input processor writes data to a packet buffer (where the adapter stores the packets in a cache, i.e. a delay register, col. 15, lines 39-43, before the packets are passed to a host memory, col. 15, lines 16-21, which contains a buffer, col. 16, lines 16-20, see also col. 14, lines 47-50).

25. Regarding claims 24 and 33, Slattery discloses that the input processor includes a host processor interface (col. 15, lines 61-64, where the adapter, i.e. input processor, communicates with a host processor, ref. 160, such that the adapter includes a host processor interface).

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26. Regarding claims 29 and 37, Slattery discloses that the input processor accepts or discards input packet data using said packet identifier table (Fig. 2 and col. 14, lines 54-64, where each input port also has a cache which stores a PID filter map, i.e. packet identifier table, which the data link control circuit uses to determine which transport packets to retain, see also col. 15, lines 32-39).

27. Claims 9, 12, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slattery et al. (USPN 6,111,896) as applied to claims 1, 2, and 11 above, and further in view of Anderson et al. (USPN 5,905,713).

28. Regarding claims 9, 12, and 25, Slattery does not expressly disclose that at least one of the input processors is a field programmable gate array. However, Slattery does disclose implementing the adaptor as a processor (col. 14, lines 24-30). Anderson teaches, in a system for processing received packets, that a field programmable gate array (FPGA) is an equivalent form for an input processor (col. 5, lines 63-67, where the analyzer is, as broadly defined, an input processor). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the input processor as an FPGA, where an FPGA is an equivalent form for implementing processing logic, depending on the constraints of the system.

29. Claims 10, 13, 38, 40-43, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slattery et al. (USPN 6,111,896) in view of Van Den Heuvel (USPN 6,175,577).

30. Regarding claims 10 and 13, Slattery discloses an input processing device for use in a re-multiplexing module that processes input packet data, comprising: an input interface that receives the input packet data (where the remultiplexer shown in Figs. 1 and 2 receives a

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plurality of data transport streams, col. 12, lines 58-65, at an interface that “selectively extracts only particular ones of the transport packets from a TS,” col. 9, lines 49-52, and where the transport streams each contain input packet data, col. 3, lines 44-45); an input processor coupled to the input interface to receive input packet data therefrom and write data to a packet buffer (where each input port has an adapter, i.e. input processor, see Fig. 2, which contains a data link control circuit, col. 17, lines 59-64, where the data link control circuit receives input packet data from a respective data transport stream, col. 15, lines 32-39, and which writes data to a host memory, col. 15, lines 16-19, containing a packet buffer, col. 16, lines 16-20); and a packet identifier table coupled to the input processor (Fig. 2 and col. 14, lines 54-64, where each input port also has a cache which stores a PID filter map, i.e. packet identifier table, which the data link control circuit uses to determine which transport packets to retain, see also col. 15, lines 32-39).

Slattery does not expressly disclose that the packet identifier table is divided into an active table containing values used by the input processor to select packets for storage in an input packet data stream and a pending table containing values that can be modified by the host processor while the active table is being used by the active table. However, Slattery does disclose that the packet identifier table is updated (col. 15, line 64-col. 16, line 2). Van Den Heuvel teaches, in a system for updating PID tables, having an active table and an update table (col. 5, lines 30-36) where it is implicit that this allows the system to continuously operate. It would have been obvious to one of ordinary skill in the art at the time of the invention to divide the packet identifier table into an active table containing values used by the input processor to select packets for storage in an input packet data stream and a pending table

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containing values that can be modified by the host processor while the active table is being used by the active table in order to permit continuous use of the filter.

31. Regarding claim 38, Slattery in view of Van Den Heuvel does not expressly disclose that the input processor includes a program clock reference detector that checks the input packet data for a valid program clock reference field. However, Slattery does disclose that each input processor obtains a reference time and records this time along with the packet (col. 15, lines 43-49). Slattery also discloses that the output processors check to see if packets have a valid PCR (col. 15, lines 56-60). Slattery further discloses that PCRs are crucial to proper recovery of the information stream (col. 3, lines 26-34). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor check the packet data for a valid program clock reference field to ensure that the system does not operate on a corrupted PCR, where a corrupted PCR could distort the decoded information stream.

32. Regarding claim 40, Slattery in view of Van Den Heuvel discloses that the input processor includes a data delay register that delays the input packet data before the input processor writes data to a packet buffer (where the adapter stores the packets in a cache, i.e. a delay register, col. 15, lines 39-43, before the packets are passed to a host memory, col. 15, lines 16-21, which contains a buffer, col. 16, lines 16-20, see also col. 14, lines 47-50).

33. Regarding claim 41, Slattery in view of Van Den Heuvel discloses that the input processor includes a host processor interface (col. 15, lines 61-64, where the adapter, i.e. input processor, communicates with a host processor, ref. 160, such that the adapter includes a host processor interface).

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34. Regarding claim 42, Slattery in view of Van Den Heuvel does not expressly disclose that the input processor checks a length of each packet of said packet data received and discards packets of incorrect length. However, Slattery does disclose that each transport packet is a fixed length (col. 3, lines 12-14). It is implicit that any packet arriving at the input processor that is a length other than the fixed length is a corrupted packet, i.e. the packet has been corrupted during transport, which has resulted in the packet having a length other than the given length. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor check a length of each received packet and to discard packets of an incorrect length in order to ensure that any corrupted packet is discarded.

35. Regarding claim 43, Slattery in view of Van Den Heuvel does not expressly disclose that, if the input processor discards a packet of incorrect length, an error bit is set that is readable by a host processor and indicates that a packet of incorrect length was discarded. However, Examiner takes official notice that it is well known in the art to signal to a processor when a packet has been discarded in order to permit the processor to collect error statistics. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor set an error bit that is readable by a host processor when it discards a packet of incorrect length in order to permit the processor to collect error statistics.

36. Regarding claim 45, Slattery in view of Van Den Heuvel discloses that the input processor accepts or discards input packet data using said packet identifier table (Fig. 2 and col. 14, lines 54-64, where each input port also has a cache which stores a PID filter map, i.e.

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packet identifier table, which the data link control circuit uses to determine which transport packets to retain, see also col. 15, lines 32-39).

37. Claims 19, 28, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slattery et al. (USPN 6,111,896) as applied to claims 1, 2, and 7 above, and further in view of Komi et al. (USPN 6,477,185).

38. Regarding claims 19, 28, and 36, Slattery does not expressly disclose that each of said packet identifier tables list packet identifiers for packets of data which are to be given priority and be processed before non-priority packets of data. Komi teaches, in a MPEG system, giving priority to certain PIDs over other PIDs in order to allow packets to be processed according to data type rather than order of arrival (col. 10, lines 47-52, see also col. 10, lines 62-65).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have the packet identifier tables list packet identifiers for packets of data which are to be given priority and be processed before non-priority packets of data in order to allow packets to be processed according to data type rather than order of arrival.

39. Claims 22 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slattery et al. (USPN 6,111,896), as applied to claims 21 and 30 above, and further in view of Magee et al. (USPN 6,002,687).

40. Regarding claims 22 and 31, Slattery does not expressly disclose that said input processor flags packets of data that include a valid program clock reference field. However, Slattery does disclose that PCRs are only inserted into selected transport packets (col. 3, lines 29-34). Magee discloses that “the adaptation field [of a transport packet carrying a PCR] will have a PCR_flag set to indicate that a PCR is present” (col. 15, lines 9-14). Therefore, it would

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have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor flag packets of data that include a valid PCR in order to signal to the system that this packet contains a PCR at a given offset location.

41. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Slattery et al. (USPN 6,111,896) in view of Van Den Heuvel (USPN 6,175,577), as applied to claim 38 above, and further in view of Magee et al. (USPN 6,002,687).

42. Regarding claim 39, Slattery in view of Van Den Heuvel does not expressly disclose that said input processor flags packets of data that include a valid program clock reference field. However, Slattery does disclose that PCRs are only inserted into selected transport packets (col. 3, lines 29-34). Magee discloses that “the adaptation field [of a transport packet carrying a PCR] will have a PCR_flag set to indicate that a PCR is present” (col. 15, lines 9-14).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the input processor flag packets of data that include a valid PCR in order to signal to the system that this packet contains a PCR at a given offset location.

43. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Slattery et al. (USPN 6,111,896) in view of Van Den Heuvel (USPN 6,175,577), as applied to claim 10 above, and further in view of Komi et al. (USPN 6,477,185).

44. Regarding claim 44, Slattery in view of Van Den Heuvel does not expressly disclose that said packet identifier table lists packet identifiers for packets of data which are to be given priority and be processed before other, non-priority packets of data. Komi teaches, in a MPEG system, giving priority to certain PIDs over other PIDs in order to allow packets to be processed according to data type rather than order of arrival (col. 10, lines 47-52, see also col. 10, lines 62-

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65). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have the packet identifier tables list packet identifiers for packets of data which are to be given priority and be processed before non-priority packets of data in order to allow packets to be processed according to data type rather than order of arrival.

Conclusion

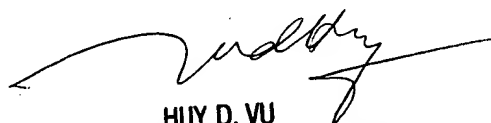
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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